ARTIFACT SHEET

Enter artifact number below. Artifact number is application number + artifact type code (see list below) + sequential letter (A, B, C .). The first artifact folder for an artifact type receives the letter A, the second B, etc.. Examples: 59123456PA, 59123456PB, 59123456ZA, 59123456ZB

_09648153   BA_

Indicate quantity of a single type of artifact received but not scanned. Create individual artifact folder/box and artifact number for each Artifact Type.

☐ CD(s) containing:
    computer program listing
    Doc Code: Computer
    ☐ Artifact Type Code: P

    pages of specification
    and/or sequence listing
    and/or table
    Doc Code: Artifact
    ☐ Artifact Type Code: S

    content unspecified or combined
    Doc Code: Artifact
    ☐ Artifact Type Code: U

☐ Stapled Set(s) Color Documents or B/W Photographs
    Doc Code: Artifact   Artifact Type Code: C

☐ Microfilm(s)
    Doc Code: Artifact   Artifact Type Code: F

☐ Video tape(s)
    Doc Code: Artifact   Artifact Type Code: V

☐ Model(s)
    Doc Code: Artifact   Artifact Type Code: M

☒ Bound Document(s)
    Doc Code: Artifact   Artifact Type Code: B

☐ Confidential Information Disclosure Statement or Other Documents marked Proprietary, Trade Secrets, Subject to Protective Order, Material Submitted under MPEP 724.02, etc.
    Doc Code: Artifact   Artifact Type Code X

☐ Other, description: _____
    Doc Code: Artifact   Artifact Type Code: Z

March 8, 2004

The United States of America

The Commissioner of Patents and Trademarks

Has received an application for a patent for a new and useful invention. The title and description of the invention are enclosed. The requirements of law have been complied with, and it has been determined that a patent on the invention shall be granted under the law.

Therefore, this

United States Patent

Grants to the person(s) having title to this patent the right to exclude others from making, using, offering for sale, or selling the invention throughout the United States of America or importing the invention into the United States of America for the term set forth below, subject to the payment of maintenance fees as provided by law.

If this application was filed prior to June 8, 1995, the term of this patent is the longer of seventeen years from the date of grant of this patent or twenty years from the earliest effective U.S. filing date of the application, subject to any statutory extension.

If this application was filed on or after June 8, 1995, the term of this patent is twenty years from the U.S. filing date, subject to any statutory extension. If the application contains a specific reference to an earlier filed application or applications under 35 U.S.C. 120, 121 or 365(c), the term of the patent is twenty years from the date on which the earliest application was filed, subject to any statutory extension.

Bruce Lehman

Commissioner of Patents and Trademarks

Andrew J Morton

Attest

[54] LIQUID CRYSTAL DISPLAY DEVICE

[75] Inventor: Jun Koyama, Kanagawa, Japan

[73] Assignee: Semiconductor Energy Laboratory Co., Ltd., Kanagawa, Japan

[21] Appl. No.: 362,881

[22] Filed: Dec. 23, 1994

[30] Foreign Application Priority Data

Dec. 27, 1993 [JP] Japan 5-354091
Dec. 27, 1993 [JP] Japan 5-354092

[51] Int. Cl.⁶ G09G 3/36; G02F 1/13
[52] U.S. Cl. 345/98; 345/92; 345/89
[58] Field of Search 345/89, 100, 92, 345/98, 90; 359/79, 56, 87

[56] References Cited

U.S. PATENT DOCUMENTS

4,773,738 9/1988 Hayakawa et al. 359/56
5,091,722 2/1992 Kitajima et al. 345/90
5,200,846 4/1993 Hiroki et al. 345/92
5,225,823 7/1993 Kanaly 345/89
5,349,366 9/1994 Yamazaki et al. 345/92
5,424,752 6/1995 Yamazaki et al. 345/92
5,471,225 11/1995 Parks 345/98
5,479,283 12/1995 Kaneko et al. 359/79
5,642,129 6/1997 Zavracky et al. 345/92

Primary Examiner—Mark R. Powell
Assistant Examiner—John Suraci
Attorney, Agent, or Firm—Sixbey, Friedman, Leedom & Ferguson, P.C.; Gerald J. Ferguson, Jr.

[57] ABSTRACT

In an active matrix type liquid crystal display device, a time gradation display manner for performing time gradation display is used. A digital gradation (voltage) signal on a signal line is supplied to the digital memory circuit arranged in vicinity of each pixel electrode and stored therein for a desired period of time. This storage state is held until next scanning is started. A high voltage or a low voltage supplied as a power source voltage of the digital memory circuit is applied to a pixel electrode while the digital memory circuit is in a storage state, so that a desired voltage is stably applied to the pixel electrode.

29 Claims, 8 Drawing Sheets